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### **EUROPEAN PATENT APPLICATION**

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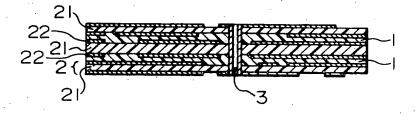
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- (54) Multilayer printed wiring board.
- A multilayer printed wiring board comprising a plurality of interlaminar insulating layers, a plurality of insulating circuit boards having circuits formed on the insulating substrates, and via holes for making electrical connection between two or more layers of circuits, wherein the difference between the glass transition point of an interlaminar insulating layer and that of the adjoining insulating substrate is not greater than 60°C, is proof against exfoliation due to heat history of the board and has high reliability of insulation and through-hole connection.

FIG.



#### BACKGROUND OF THE INVENTION to import adjusted seeds to be use

The present invention relates to a multilayer printed wiring board, particularly one used for semiconductor chip package, and a process for producing such a wiring board. Package and a process for producing such a wiring board.

Multilayer printed wiring board usually comprises an insulating substrate, a power layer, a ground layer, circuit conductors formed on the surface thereof, inner layer circuits, via holes or through-holes for making electrical connection of the circuits in the respective layers, and solder resists for insulating the surface circuits.

Warious methods are available for the manufacture of multilayer printed wiring boards such as mentioned above. For example, a method is popularly known which comprises forming the inner circuits and interlayer foil of a copper-clad laminate, placing thereon a prepreg and a copper foil in layers, integrally laminating them by heating under pressure, forming openings at the parts where electrical connection is to be made, metallizing the inner walls of said openings by electroless plating or other means, etching away the unnecessary parts of the copper foil on the surface, then coating a solder resist thereon and drying the same.

with the respective layers are formed sepaor, which rately and positioned by using guide; pins, and after, integral lamination, the through-holes, outer layer circuits or and solder resist are formed, and the recovered and separate the product of the respective layers are formed.

Regarding semiconductor chip packages, Japanese Patent Application Kokai (Laid-Open) [JP-A-] No. 59-14-58579 discloses aleadless chip carrier in which the terminals connected to semiconductor chips are extended 20 out from the inside to a part on the outside of the package.

a plurality of terminal pins for connection to the through-holes in other package-carrying wiring boards, and a plurality of terminal pins for connection to the through-holes in other package-carrying wiring boards, and a process for producing such an array. This patent also presents a ball-grid array in which solder balls are fused to the lands instead of pins in the pin grid array to make electrical connection by soldering.

. காலம் p.25je நாள் JP,-B-58-26828 discloses a tape automatic carries constituted by first forming the terminal strips and then insulating them with a tape-like insulating films was நிக்கும் எறுக்கு நடித்து நடித்து நடி

terial has been used for insulators and electrical connection of these chip carriers to semiconductor chip terminals has been made by wire bonding. Organic insulating material has been used as sealant for protecting the semiconductor chips and electrical connections from the environment after the semiconductor chips have

Recently, in view of economical disadvantages of ceramic chip carriers due to the increased number of the control of the increased number of the control of the increased number of the control of the certain the ce

Necessity has become acute recently for increased density of wiring and size reduction of wiring boards to meet the request for smaller size and functional multiplication of electronic devices. Smaller thickness is also required of the insulators used for interlayer insulation between the inner layer circuits. The conventional prepregs using woven or non-woven glass fabrics are capable of answering to such request for size reduction, and it is therefore attempted to apply an insulating resin or to use a film of insulating resin.

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ere of thread anythis phenomenon tends to occur particularly when the through-holes are formed in the multilayer wiring the own of the following many via tholes are formed in the layers containing no reinforcement such as woven or non-containing the following many in the layers containing the reinforcement such as woven or non-containing the following particular and the second containing the following particular and the second containing the containing the following particular and the following particula

## Distribution of the most relief of the second of the secon

exfoliation of laminations due to heat history of the board and has high reliability of insulation and electrical econnection by through-holes, and a process for producing such a multilayer printed wiring board.

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The present invention provides a multilayer printed wiring board comprising a plurality of interlaminar insulating layers, a plurality of insulating substrates containing a reinforcement, circuits formed on the surfaces of said insulating substrates, and via holes for making electrical connection between at least two layers of circuits, wherein said via holes run through the two layers of insulating substrates and the interlaminar insulating layers being the layers not containing a reinforcement, and further characterized in that the B-stage resin flow of said insulating layers is less than 1%, and

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that the difference between the glass transition point of said interlaminar insulating layer and that of the insulating substrate adjacent thereto is not greater than 60°C.

'The present invention also provides a process for producing a multilayer printed wiring board, which comprises integrally laminating, by heáting under pressure; B-staged interlaminar insulating layers and insulating circuit boards having circuits formed on the reinforcement-containing insulating substrates, and forming via holes for electrical connection between two or more layers of circuits, wherein said via holes run through two 🔭 🗥 läyers of insulating substrates and the interlaminar insulating layer disposed therebetween, said interlaminar insufating layers being the insulating layers not containing a reinforcement, and further characterized in that the B-stage resin flow of said insulating layers is less than 1%, and that the difference between the glass tranto slition porint of said interlaminar insulating layer and that of the insulating substrate adjacent thereto is not great-‴ gndi or " er than 60°C. 24 MED 20 19 4- 2344 51 15.1

### BRIEF DESCRIPTION OF THE DRAWINGS (3.110). The California was a second

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ি এক জিলাৰ ক্ষালিক প্ৰায়ে বিজ্ঞান কৰি diagrammatic sectional view for illustrating the structural features of the present invention. 48 FIGS 2A to 2C are diagrammatic sectional views for illustrating an example of use of the present invention.

Juditation of Standard and Com-

FIG. 3 is a diagrammatic sectional view showing a mode of practice of the present invention.

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11 Mall of FIGS 4A and 4B are diagrammatic sectional views for illustrating the process of the present invention.

FIGS: 5A to 5C are diagrammatic Sectional Views showing another mode of practice of the present inven-Let all the parties of their factorials and the parties of tion.

the state of the present FIGS: 6A to 6G are diagrammatic fragmentary sectional views for illustrating the structure of the present E have a head officention. The respectable in a feet apply at left of the first out of each begin the continued in

the resent inverificity to lytting income a techtuale eligible year or and an englicible technical and of

'FIGS.'8A to 8E are diagrammatic sectional views for illustrating the respective steps in the process according to an embodiment of the present invention, the later the difference of the later to guidalistic

and the state of t The Charlet of the Cordina to another embodiment of the present invention; see the content of the content of the present invention.

para - mg not in 🕒 FIG. 10 is a diagrammatic sectional view showing still another embodiment of the present invention.

ি প্রান্তির কালি Figs: শার্মি to বিটার্লিল diagrammatic sectional views for illustrating the prior art problems.

FIGS. 12A to 12G are diagrammatic sectional views for illustrating an example of production process acto make a sectionality and the present invention: I be the security and the contract to well and the contract the contract to the contract to

Tanting and FIGS. 13A to 13G are diagrammatic sectional views for illustrating another example of production process കണ്ടാലെ ചാന് laccording to the present invention, ne ഉണ്ടാടെ ശന്ദ്രനടെ പ്രവാധ കാരവാ നടരെ ഉറയാന് പ്രദ്യാത ¥ .

FIGS. 14A to 14D are diagrammatic sectional views for illustrating still another example of production procaccording to the present invention, we say that the amount of the present invention, we say that the say that the say the say that the say the say that the say the say that the say the to new the acceptable increases seen the monoral resident of the later of the later after their new terms and the later after their new terms after their new terms after their new terms and the later after after the later after the later after the later after the later

The discrete PIDESCRIPTION OF THE PREFERRED EMBODIMENTS of article fall and the breath in breath a section aize read that The committee of the content to the Section and Section by the content of the con

The multilayer printed wiring board according to the present lavention comprises a plurality of interlaminar તા મોર્ડ માં 🖰 મારા પ્રવાસ (ng layers, a plurality of insulating substrates containing a reinforcing material and laminated alternately, circuits formed on the surfaces of said insulating substrates, and via holes for making electrical connection between two or more layers of circuits, wherein said via holes run through two layers of insulating substrates 🐃 🖘 😘 😘 and the interlaminar insulating layer formed therebetween, said interlaminar insulating layers being the insu-1963 To 1945 We liating layers not containing a reinforcement, and further characterized in that the Bastage resin flow of said insulating layers is less than 1%, and that the difference between the glass transition point of the interlaminar insulating layer and that of the insulating substrate adjacent thereto is not greater than 60°C.

Regarding the materials of the interlaminar insulating layers and the adjoining insulating substrates used in the present invention, the glass transition point of these materials is investigated and those having the above-்க்க 🤚 55 சி défined difference (not greater than 60°C) in glass transition point are selected and used for the adjoining lamwhich is the control of the difference in glass transition point is preferably not greater than 40°C and the control of the co

the street of the transfer of the street of 10.3 x 80.65 x 30 différence in glassifransition point between the one with the highest glass transition point and the one with The first of the lowest glass transition point is not greater than 30°C, and the their services are various.

🐃 🖖 15 55 041 165 Since no reinforcing fiber is contained in the interlaminar insulating layers, it is desirable that the insulating m Butter die er missbetrates used in the present invention comprise reinforcing fiber such as glass cloth, glass paper, glass short security as a sufficiency the like impregnated with an appropriate resin such as epoxy resin, polyimide resin or the like for inthe all the hibiting change of size due to heat history in the course of working.

In case of using a polymeric epoxy-type adhesive film AS-3000 (trade name, available from Hitachi Chemical Co., Ltd.) for the interlaminar insulating layers, since the glass transition point of this insulator is 105-130°C, the material usable for the insulating substrates disposed adjacent to said respective insulating layers is one having a glass transition point of 70-165°C. Examples of such material are a polymeric polyimide-type adhesive film AS-3000 (mentioned above), an epoxy resin-imprognated prepreg GEA-67 (trade name, available from Hitachi Chemical Co., Ltd.) and an epoxy solder resist CCR-506(trade name, available from Asahi Chemical Laboratory, Ltd.).

In case of using a polyimide-type adhesive film AS-2250 or 2210 (trade name, available from Hitachi Chemical Co., Ltd.) for the interlaminar insulating layers, since the glass transition point of this insulator is 165-170°C; the material usable for the adjoining insulating substrates is one having a glass transition point of 110-225°C. Examples of such material are a polyimide-type adhesive film AS-2250 or 2210 (mentioned above), an epoxy resin-impregnated prepreg GEA-679 (trade name, available from Hitachi Chemical Co., Ltd.) and a heat resistant thermosetting BT resin (containing triazine component and bismaleimide component as fundamental components)-type prepreg GHPL-830 (trade name, available from Mitsubishi Gas Chemical Co., Ltd.).

In case of using an epoxy solder resist CCR-506 (mentioned above) for the interlaminar insulating layers, since the glass transition point of this insulating material is 100-115°C, the material usable for the adjoining insulating layers is one having a glass transition point of 55-160°C, such as an epoxy solder resist CCR-506 (mentioned above), a polymeric polyimide-type adhesive film AS-3000 (mentioned above), an epoxy resin-impregnated prepreg GEA-67 (mentioned above) and the like.

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When insulating material of the same system is used for both of the interlaminar insulating layers and insulating substrates, there is no other alternative but to apply said material in the state of varnish on the surface of the insulating circuit board. In this case, as it is required to satisfy both requirements of controlled coating thickness and reduction of coating thickness at the same time, there are involved technical difficulties and complication of the production process.

For such control of coating thickness and reduction thereof, there can be used solder resist ink generally employed in the manufacture of wiring boards, and the type of ink to be used can be properly selected in conready sideration to the above-defined range of glass (transition point, pages) and laten range in

More preferably, a varnish is applied on the support film and dried into an adhesive film so that said layers

consistency to can be used in the Bratage state, to it bearing who begins and bearingst along the say entailed 30 As for the properties of said interlaminar insulating layers containing no reinforcement such as weven or nonwoven glass fabrics, it is desirable that the B-stage resin flow of said layers is less than 1%, and the Bstage viscoelasticity of said layers is in the range of 2,000-5,000 MPa at 30°C and in the range below 10 MPa in many to at the molding temperature, and it has the members of project on taken must be out hid one

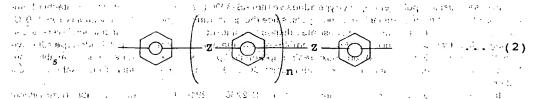
The layer materials satisfying these requirements include polymeric epoxy film, polyimide film and epoxy solder resist ink. As the film in the state of B stage, there can be used, for example, such commercial products as AS-3000 (polymeric epoxy adhesive film) and AS-2250 and 2210 (polyimide adhesive film, both mentioned above).

As the polyimide adhesive film material, there can be used a thermosetting resin comprising 40-70% by weight of a polyimide having the structure represented by the following formula (1), 14-45% by weight of a 40 ... bismalejmide-diamine reaction product and 15-45%, by weight of an epoxy resing the second

wherein Ar is a group represented by the following formula (2) or (3), the group of the formula (2) being contained in an amount of 10-98% by mole and the group of the formula (3) being contained in an amount of 90-5% by ുള്ള പ്ര**55**നും **mole;** പ്രവേദ്യവും in the first transfer of the protection production in the bridge forms of

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wherein Z represents -C(=0)-, -SO<sub>2</sub>-, -O-, -S-, -(CH<sub>2</sub>)<sub>m</sub>-, -NH-C(=O)-, -C(CH<sub>3</sub>)<sub>2</sub>-, -C(CF<sub>3</sub>)<sub>2</sub>-, -C(=O)-O- or a ່ ທີ່ ທີ່ທີ່ປ່າໄດ້ຕີວ່າ ໄດ້ຕີດີ mare each an integer of 1 or greater; Z's may be the same or different from each other, and each hydrogen in each benzelle ring may be substituted with an appropriate substituent; , ac . . . . .

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சூர்கள் 🔭 ி whierein R1, R2 R3 and R4 represent nidependently hydrogen, C42, alkyl group, or alkoxy group, with at least two of them being alkyl group of alkoxy group; and X represents CH2-, C(CH3)2- 40-, -SO2-, -C(=0)- or -NH-าง เออสาโดง หารีโดงเรียก ถึง เดา C(=O)-.

1 li. 34 -25 1 ... -'For producing a multilayer printed wiring board such as described above, as shown in FIG. 1, a plurality of B-staded interlaminar insulating layers 1 and insulating substrates 21 are selected so that the difference in glass transition point between the adjoining insulating layers will fall in the range not exceeding 60°C and said interlaminar insulating layers and insulating circuit boards 2 having circuits 22 formed on the insulating substrates are integrally laminated by heating under pressure, and then via holes for making electrical connection between two or more layers of circuits are formed. Said via holes run through two layers of said insulating sübsträtes and the interiaminar institating layer disposed therebetween. Said interfaminar insulating layers are the insulating layers containing no reinforcement such as woven or nonwoven glass fabrics: Also, the B-stage resin flow of said insulating layers is less than 1%, and the difference in glass transition point between an insulating layer and the insulating substrate adjacent thereto is not greater than 60°C.

35 Such a multilayer printed wiring board can also be produced according to the following processes (a)-(d). in is to measurement Charly Commercial speak adhesive in the 1979 and 2270 in Spinite all

and colving the bill feet is the proceeding the color of boiles the diameter (1996).

#### Process (a) vit "(" the minima

or the horastic y in the First, etching resists are provided at the parts where circuits are to be formed on a laminate comprising copper-clad insulating substrates containing reinforbing fiber, such as shown in FIG: 12A, to constitute an insulating circuit board as shown in FIG. 12B. There are prepared at least two insulating circuit boards described above. Between these insulating circuit boards is disposed an interlaminar insulating layer which is in the state of B stage and contains no reinforcing fiber and in which the B-stage resin flow is less than 1% and the difference in glass transition point between this layer and the adjoining insulating substrate is not greater than 60°C (FIG. 12C). These insulating circuit boards and insulating layers are laminated by heating under pressure as shown in FIG. 12D, and solder resists are provided over the whole surfaces of the integral multilayer laminate as shown in FIG. 12E. Then holes are formed by a drill to the section where electrical connection is required, as shown in FIG. 12F, and a conductor layer is formed on the inside of each of said holes by electroless plating, thereby producing a multilayer wiring board as shown in FIG. 12G. Formation of holes down to the necessary section for connection can be accomplished by driving a revolving drill down to the depth of the layer to be connected, stopping further driving of the drill at this point and returning it to the initial position.

ந்து நார்க் அரசு **Process (b)** பிரிக்குள்ளுள்ளும் இருந்திரும். சிருந்திரி சிருந்தை நடிக்க விருந்த இருந்திரும். Talling digital transport of the second search agreement to be suit to be March 2010 Programmer and the Million

> No circuit working is performed on the outermost side of the insulating circuit board constituting the outermost layer of the laminate consisting of copper-clad insulating substrates containing reinforcing fiber such as shown in FIG. 13A, and etching resists are formed at the parts which are to become circuits. The unnec

D.C

, essary copper foil is etched away to make an insulating board shown in FIG. 13B. There are prepared at least two such circuit boards. At least between these circuit boards is disposed an interlaminar insulating layer which is in the state of B stage and further characterized by the facts that the B stage resin flow is less than 1%, with the difference in glass transition point between the adjoining insulating layers being not greater than 60°C (FIG. 13C), and that said circuit boards and insulating layers are laminated by heating under pressure as shown are in FIG. 13D. Holes are formed in the obtained laminate to a depth necessary for connection as shown in FIG. 13E. A conductor layer is formed by electroless plating as shown in FIG. 13F. Then etching resists are formed on the outermost copper-clad surfaces, and the unnecessary copper is etched away as shown in FIG. 13G. 1.38 Carte of the Ba green range to the Villa

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Process (c) 1998 10 V

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26.6 0.73.00 Charleston, Bridge Co. Etching resists are formed at the pertinent parts (for forming circuits) of a laminate consisting of copperclad insulating substrates containing reinforcing fiber, and the unnecessary copper foil is etched away to form an insulating circuit board. There are prepared a pair of such insulating circuit boards. Between these insulating circuit boards is sandwiched an interlaminar insulating layer which is B-staged and specified by the facts that its B-stage resin flow is less than 1%, that the difference in glass transition point between the adjoining insulating layers is not greater than 60°C, and that this layer contains no reinforcing fiber. These circuit boards and or a significant insulating layers are laminated by heating under pressure, holes are formed in the laminate, and conductor layers are formed by electroless plating to make an interlayer circuit board. There are prepared at least two 13 to 1800 as such interlayer circuit boards, and between these interlayer circuit boards is disposed an interlaminar insulating has a Bestaged, has a Bestage resin flow of less than 1%, with the difference in glass transition point between the adjoining insulating layers being not greater than 60°C, and contains no reinforcing fiber. These De the standard procedure and insulating layers are laminated by heating under pressure plated resists are formed over the surfaces of the laminate, holes are formed in the laminate by drilling, and conductor layers are further 25 of formed by electroless plating the weath and heaven between mile or an even and a manner thomas with a super-section (3) is a record contained by the some powers, and a contained consequent and all a consequences of the

happy (12.3 file. Process.(4)) again a his traffic belong a second restly note. In 18 Shesoxe algebra, confining

than the perchant to since an account one of the great medited be Hill a subsequent tribe within an Two interlaminar circuit boards such as shown in FIG, 14A are made according to the process (c) described 30 above. Between these circuit boards is disposed an interlaminar insulating layer which is 8 staged, has a 8stage resin flow of less than 1%, with the difference in glass transition point between the adjoining insulating and contains no reinforcing fiber, as shown in FIG. 14B. They are integrally laminated by heating under pressure, and as shown in FIG. 14C, holes are formed by drilling in the laminate to a depth reaching the section where electrical connection is required. Then, as shown in FIG. 14D, conductor layers are formed by electroless plating, etching resists are formed to the shape of the circuits in the outermost the property layer, and unnecessary copper feil is etched away the letter to the control of the control of the

In at least one of the interlaminar insulating layers 1, or insulating substrates 21 in said multilayer wiring board are formed cavities 4 for housing the semiconductor chips to be mounted later, as shown in FIG. 2A, to provide a multilayer wiring board for chip carrier, the fiber this alternate out to en dan one it

nic 40 to an a Conventional methods can be used for forming said cavities. Preferably, the cavities are enlarged in size successively from the one in the insulating layer closest to the location where a semiconductor chip is to be set as shown in FIG. 2B, and terminals for making electrical connection with the semiconductor chips to be mounted later are provided in the circuits formed on the surfaces of the interlaminar insulating layers or semiconductor substrates exposed by the respective cavities, thereby

19 10 10 45 ven providing a chip carrier with many electrical connections. The rest of the connections at the A chip carrier with high heat radiating efficiency, can be obtained by providing a heat sink 5 arranged to close one of the openings 42 of the cavity formed as a through hole as shown in FIG. 2C.

spons) ലി പട്ടെ പ്രദ്നീhis heat sink 5 may be designed to consist of a support portion 51 for carrying a semiconductor chip and a brim 52 provided around said support portion and smaller in thickness than the support portion as shown in total and a second section of the heat, sink is fitted in an opening formed in the outermost one of the interlain the state of the seminar insulating layers or insulating substrates, said opening being substantially same in size as said support control of apportion of the heat sink. The insulating substrates having circuits formed thereon are placed on said heat sink and integrally laminated by heating, under pressure, and then, via holes for making electrical connection between two or more layers of circuits are formed. It is thereby possible to accomplish attachment of the heat ng grad in 55 sydisink and laminate molding of the chip carrier at the same time, you become in the page of the

construction of the Adhesive strength of the heat sink can be increased by forming a pertinent unevenness on the surface of at least the brim:portion 52 of the heat, sink to be attached to an insulating layer, as the second

chips to be mounted later are formed in at teast one of the interlaminar insulating layers or insulating substrates, and the laminating members are placed where on the other successively in the order of flat panel/protective film/combination of Bustaged interlaminar his detining flayers and insulating substrates having circuits/cushion material/molded article having holes of the said mile size as cavities/flat panel, and they are integrally laminated by heating under pressure, as shown in Fig. 4A.

For attaching the heat sink simultaneously with laminate molding of the chip carrier, the laminating members are placed in the order of flat panel/cushion material/plastic film low in melting point and high in flow at heating temperature for lamination (e.g. polyethylene film)/protective film high in melting point and flexible at heating temperature for lamination/combination of B-staged interlaminar insulating layers and insulating substrates having circuits/cushion material/molded article having holes of the same size as cavities/flat panel.

In this chip carrier, terminals for making electrical connection with other wiring boards are provided on one to the conductor chips may be provided on the same side or on the opposite of the conductor chips may be provided on the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the same side or on the opposite of the conductor chips may be provided in the conductor chips may be p

Union of the When a plurality of pins are ชื่อยd as terminals for making electrical connection with other wiring boards ใน 100 รีร์ย Yas shown in FIG. 5A, a pin grid array package is provided. When lahlds are formed for electrical connection by แก้กเลือน เชียง of solder balls as terminals for making electrical connection with other wiring boards as shown in FIG. 5B, a provided that a provided the formed for the connection with other wiring boards as shown in FIG. 5B, a provided that a provided the formed for the connection with other wiring boards as shown in FIG. 5B, a provided that the connection with other wiring boards as shown in FIG. 5B, a provided that the connection with other wiring boards are connected as the connection with other wiring boards.

The process has a state is also possible to form a chip-on-chip wirling board on a multi-chip module by combining said arrays as the shown in FIG. 5C.

the present inventors found that when the internaminar insulating layers contain no reinforcement such as woven of the present inventors found that when the internaminar insulating layers contain no reinforcement such as woven of his present in the internation of voids and the internation of the internation in internation in internation of the internation of the internation of the internation in internat

If the difference in glass transition point between said interlaminar insulating layer and the adjoining insulating substrate exceeds 60°C, when the laminate is cooled after heat curing, the material with high glass transition point is perfectly solidified but the material with low glass transition point does not lose its fluidity and the laminate, consequently affarge stress is built up in the laminate, and between the through-holes of the interlaminar insulating layers at the parts where the through-holes of via holes and are present in close order.

னிய சூர் சிரி More specifically, the multilayer Willing board of the above structure is subject to the following undesirable முதல் சிரி phenomena as illustrated in Fig. 11! உருகள் கொள்ள நடிகள்கள் நடிகள்கள்

- າກ ກະການ ປະຕິທີ (1) Movement of the substrate in the thickness direction is restricted by through holes or via holes (FIG.
- (2) Due to this restriction, when the lamiffate is heated, the whole insulating layer swells up to the form of the whole insulating layer swells up to the whole insulating layer swell up to the whole insulating layer swell
- temperature of the material with high glass transition point (FIG. 11C); act that a decorpt (4) The material with low glass transition point is still obtained to restore its original shape even when the college of the first time is the college of the college
- ਬੁਲਮਾਈ ਫ਼ਰਮਿੰਡਰ ਤੇ ਪ੍ਰੰਤੇ) Exfoliation and formation of voids are caused by the targe stress (FIG: 11D). ਪਿਸਤੀ ਨ
- The present invention has been attained on the basis of the above disclosure and especially features the about the interlaminar insulating layer and that of the interlaminar insulating layer and that of the adjoining insulating substrate whot greater than 60°C; there is produced no large stress that will cause the adjoining insulation of laminations or formation of voids. The smaller the difference, the more desirable. Said difference in the color of the more desirable and the color of the colo

in the base of a multilayer wifing board made by using a plurality of interlaminar insulating layers and inthe base sulating substrates, it is desirable that not only the difference of glass transition point between the adjoining the base of misulating layers but also the difference of glass transition point between the insulating layers used in each add to be unit of wining board be small, preferably not greater than 60°C; more preferably not greater than 40°C.

as woven or nonwoven glass fabilities to be less than 4%, it is possible to secure the required layer thickness.

3.55 as woven or nonwoven glass fabilities to be less than 4%, it is possible to secure the required layer thickness.

3.55 and 15 and 16 also, when these insulating layers are used for a chip carrier having cavities; it is possible to minimize penetration of resiminto the bavities. Further by setting the viscoelasticity of said insulating layers at 30°C to be setting to a said insulating layers at 30°C to be setting to a said insulating layers at 30°C to be said in the layers in the working proc-

ess, and by setting said viscoelasticity at the molding temperature to be in the range below 10 MPa, it is possible to secure enough laminate moldability for embedding the circuit conductors in said layers.

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usone entichent This Example is explained with reference to FIGS, 6-8 of the accompanying drawings.

(1) The side with no copper foil of a BT resin-type single-side copper-clad laminate CCH-HL 830 (trade name, available from Mitsubishi Gas Chemical Cc., 1td.) having a glass transition point of about 170°C and a thickness of 0.4 mm was subjected to spot facing to a depth of 0.2 mm to prepare a first insulating substrate 71 having a hollow such as shown in FIG. 6A.

(2) In a polyimide adhesive film AS-2250 (trade name, available from Hitachi Chemical Co., Ltd.) having ogar gradini ili a glass transition point of about 170°C and a thickness of 0.05 mm, there was provided an opening 723 greater than the spot facing working portion of the first insulating substrate to prepare first interlaminar insulating layer 72 such as shown in FIG. 6B.

(3) In a BT resin-type single-side copper-clad laminate CCH-HL 830 (trade name, available from Mitsubishi Gas Chemical Co., Ltd.) was provided an opening 735 the same in size as the opening of the first interlaminar insulating layer, and terminal 731 for making electrical connection with semiconductor chip by wire bonding was provided at the part to be exposed when a third insulating substrate is laminated at a later stage, while inner layer circuit 732 was provided at the non-exposed part to prepare a second insulating

20 substrate 73 such as shown in FIG. 6C applicate to thursday go verstanticul aurio (4) In a 0.075 mm thick polyimide adhesive film AS-2250 (mentioned above) was provided an opening 743 the same in size as the opening of the second insulating substrate to prepare a second interlaminar insulating layer 74 such as shown in FIG. 6D.

(5) In a 0.4 mm thick BT resin-type single-side copper-clad laminate CCH-HL 830 (mentioned above) was provided an opening 753 greater than the opening in the third insulating substrate to prepare a third insulating substrate 75 such as shown in FIG. 6E.

(6) In a 0.1 mm thick polyimide adhesive film AS-2250 (mentioned above) was provided an opening 763 , of the same size as the opening in the third insulating substrate to prepare a third interlaminar insulating layer 76 such as shown in EIG. 6F. 26.9 3 John Sword as 13 a raind 3

30 (7) A 0.2 mm thick BT resin-type single-side copper-clad laminate CCH-HL 830 (mentioned above) was and the second seed as a fourth insulating substrate 77, as shown in EIG, 6G.

(8) The layers obtained in (1)-(7) above were placed one over the other in that order and integrally laminated under the conditions of 20 kgf/cm<sup>2</sup>, 180°C and 180 minutes. The laminate had the structure of: flat pane! 81/protective film 82/structure 83 of (1)-(7)/cushion 84/molded article 85 with opening of the same size as cavity/flat panel 86, as shown in FIG. 7.

(9) After laminate molding, through-holes were formed (FIG. 8A), and electroless plating was carried out on the inner walls of said through-holes and the surface of the laminate (FIG. 8B), and then outer layer circuits were formed (EIG, 8C). For forming cavity, an opening of the same size as the opening in the third insulating substrate was formed at the same location, and then an opening was further formed by end milling machine at the part corresponding to the fourth insulating substrate (FIG. 8D). Finally, a plurality of pins were fixed in the through-holes to constitute a pin grid array with cavities. To

#### ം നാംപ്യാപ്പു Example,2<sub>6</sub>) സാണ്ട്രങ്ങളാണ് പ്രവീധി ഉണ്ടുവന്ന് മണ്ടാന് അവ സർക്ക് ലേണ് മാന് വേദ്യമായിരുന്ന് വിത്രന്

- error commit about 190°C and a trib brevs of our manuage prepring traveng and sense. 45 (1) An epoxy resin-impregnated copper-clad glass cloth laminate MCL-E-67 (trade name, available from Hitachi Chemical Co., Ltd.) having a glass transition point of about 120°C, and a thickness of 0.2 mm was The latest temperature of the prepared as: first insulating substrate, grant much a section of the other section to
- (2) A polymeric epoxy adhesive film AS-3000 (mentioned above) having a glass transition point of about 120°C and a thickness of 0.05 mm and provided with an opening to define a cavity was prepared as first 50 The ginterlaminar insulating layer. The properties above training to be self-or united to
- (3) In a 0.4 mm thick epoxy resin-impregnated copper-clad glass cloth laminate MCL-E-67 (mentioned above) was provided an opening of the same size as the opening in the first interlaminar insulating layer, and a terminal for connection with semiconductor chic, by wire bonding was provided at the part which is at the state of the exposed when laminated with a third insulating substrate, while inner layer circuits were provided at the commendating substrate as non-exposed part to prepare a second insulating substrate as the commendation of the
- (4) In a 0.05 mm thick polymeric epoxy adhesive film AS, 3000 (mentioned above) was provided an opening greater than the opening in the second insulating substrate to prepare a second interlaminar insulating mana agrega layer, and the broken of the general considers explanation from the agent Court of the

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(5) In a 0.4 mm thick epoxy resini impregnated copper-clad glass cloth laminate MCL-E-67 (mentioned above) was provided an opening of the same size as the second interlaminar insulating layer, and a terminal for connection with semiconductor chip by wire bonding was provided at the part which is exposed when laminated with a fourth insulating substrate, while inner layer circuits were provided at the non-exposed part to prepare a third insulating substrate. (6) In a 0.05 mm thick polymeric epoxy adhlesive film AS-3000 was provided an opening greater than the opening in the third substrate to prepare a third interlaminar insulating layer. (7) In a 0.4 mm thick epoxy resin-impregnated copper-clad glass cloth laminate MCL-E-67 was provided an opening of the same size as the third interlaminar insulating layer to prepare a fourth insulating sub-(8) In a 0.05 mm thick polymeric epoxy adhesive film AS-3000 was provided an opening of the same size ESignMear ( 00 as the opening in the fourth insulating substrate to prepare a fourth interlaminar insulating layer. chastente Parena. (9) A 0.4 mm thick epoxy resin-impregnated copper-clad glass cloth laminate MCL-E-67 was prepared as a fifth insulating substrate. inc many 15 months of (10) The layers obtained in (1)-(9) above were placed one over the other in that order and integrally lamdine hast biter inated by heating under pressure under the conditions of 40 kgf/cm², 175°C and 90 minutes. The laminate, as shown in FIG. 7, had the structure of flat panel 81/protective film 82/structure 83 of (1)-(9)/cushion 39' 11 & 13-15 Street 84/molded article 85 having opening defining cavity/flat panel 86. (11) After laminate molding, through-hotes were formed (FIG. 9A), the inner walls thereof and the surfaces of the laminate were subjected to electroless plating (FIG. 9B), outer layer circuits including lands for fu-ระที่ เกษา จะมีสุดเทอ 75.2 sion-bonding solder balls were worked (FiG. 9C), an opening of the same size as the opening in the fourth insulating substrate was formed at the same part white an opening was formed by end milling machine at the part corresponding to the fifth insulating substrate for forming cavity (FIG. 9D), and then solder resists were applied and dried to constitute a ball grid all ayect man in a constitute a ball grid all ayect man in a constitute a ball grid all ayect man in a constitute as a consti or Them I being th 19 SPE in which is now being the great Example 3

Figure 10 to 15 to 25 and a control of the control of t In Example 1, through-hole was provided instead of spot facing working portion in the first substrate, and a heat sink having a brim such as shown in FIG. 3 was prepared. The layers were laminated under the same 30 Conditions as in Example 1 except for the laminate structure of: flat panel/cushion/polyethylene film/polyimide film/structure of (1)-(7) + heat ຮໍໄກເຂົ້າໄດ້ປະກິໄວຄຳໃຫ້ດໍໄດ້ຍີ່ article with ດຸກິຍາເກີຢູ defining cavity/flat panel to constitute 3. 4 Example 4 (1) 4 (1) 4 (1) 1 (2) 1 (3) 4 (3) 1 (3) 1 (3) 1 (3) 1 (4) 1 (4) 1 (4) 1 (5) 1 (4) 1 (5 1 THE PROPERTY AND ASSESSMENT 35 (1) An epoxy resin impregnated copper-clad glass cloth laminate MCL-E-67 (mentioned above) having a glass transition point of about 120°C and a thickness of 0.2 mm was prepared as a first insulating substrate. land the transition point of about (2) In a polymetric epoxy atthesive film AS-3000 (mentioned above) having a glass transition point of about 120°C and a thickness of 0.05 mm was provided an opening defining cavity to prepare a first interlaminar insulating layer. The transfer druck at the public process of the action of (3) Two pieces of 0.1 rfim thick epoxy resid-impregnated copper-clad glass cloth laminate MCL-E-67 (mentioned above), each being provided with inner layer circuits and having via holes formed therein, were laminated by disposing therebetween an epoxy resin prepreg GEA-679 (mentioned above) having a glass transition point of about 120°C and a thickness of 0.1 mm. An opening having the same size as the opening 1000 strips to the first interlaminal insulating layer was formed in the laminate. Atterminal for connection with semiconductor thip by wire bondling was provided at the part which is exposed when laminated with a third insulating substrate, and inner layer circuits were provided at the non-exposed part to prepare a second insulating substrate. It is do hear a leady 3008 of pall the the control and the Aris, the the to think of the eration to 👫 (4) In a 0.05 mm thick polymetic epoxy adhesive film AS-3000 was formed an opening greater than the opening in the second insulating substrate to prepare a second interlaminar insulating layer. A Mediagrati Vin da-(5) Epoxy solder resists having a glass transition point of about 110°C were applied to two pieces of 0.1 mim thick epoxy resint impregnated copper clad glass cloth laminate MCL-E-67, each being provided with al-lio প্রায়ের কর্ম মার্লিটা layer circuits and flaving vie holes formed therein, and they were laminated এAn opening of the same ਕੋਮੀ ਨੂੰ ਇਕ ਮਾਮੇ ਕੀਤਾ size as the second interlaminar insulating layer was formed in the laminate. A terminal for connection to semiconductor chip by wire boriding was provided at the part exposed when laminated with a fourth insu-55

substrate; in cone of the data data government in notes on a cipilate to the head to be ag

lating substrate, and inner layer circuits were provided at the non-exposed part to prepare a third insulating

(6) In a 0.05 mm thick polymeric epoxy adhesive film AS-3000 was formed an opening greater than the

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opening in the third insulating substrate to prepare a third interlaminar insulating layer. (7) In a 0.4 mm thick epoxy resin-impregnated copper-clad glass clott laminate MCL-E-67 was formed an opening of the same size as the third interlaminar insulating layer to prepare a fourth insulating substrate. (8) In a 0.05 mm thick polymeric epoxy adhesive film AS-3000 was formed an opening of the same size as the opening in the fourth insulating substrate to prepare a fourth interlaminar insulating layer. (9) A 0.4 mm thick epoxy resin-impregnated copper-clad glass cloth laminate MCL-E-67 was prepared as stantar on her one of their indone. a fifth insulating substrate. .... (10) The layers obtained in (1)-(9) above were placed one over the other in that order and laminated under the conditions of 40 kgf/cm² 175°C and 90 minutes. The laminate had the structure of: flat panel 81/ protective film 82/structure of (1)-(9) 83/cushion 84/molded article 85 having opening of the same size as cav-. o. . en. tsubstitution of a ity/flat panel 86, as shown in FIG. 7. po e. a.c.

(11) After laminate-molding, the laminate was subjected to drilling for forming through-holes, electroless plating on the inner walls of the holes and the surfaces of the laminate, followed by electroplating, drilling The last of an opening of the same size as the opening in the fourth insulating substrate at the same part and formation of an opening by end milling machine at the part corresponding to the fifth insulating substrate for forming cavity to provide a multilayer wiring board for chip carrier such as shown in FIG. 10. The latest site measure, the Quetral transfer and reconstrict setting as a transfer

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Constitution

are negricos reducirA multilayer wiring board, was produced by following the same procedure as Example 1 except that an 3 pril slope, epoxy solder resist ink CCR-506 (trade name, available from Asahi Chemical Laboratory, Ltd.) having a glass a see, 1881, transition point of 100-1155C was used for the second interlaminar insulating layer. The distribution of the order of the superstance of the contract of the contra

r aya. cur 6't su 🦈 aliene ∧ maiComparative Example 2-கம்! ஓமலைில்ன ஒன்க மல் கட்டக்க பிரிச் நகட் புரிவைத் பொறுகள்

section 25mile in new message months incomes any mention perform six common the conversion of the A multilayer wiring board was produced by following the same procedure as Example 2 except that a polyimide resin-impregnated copper-clad glass cloth laminate MCL-I-671(rade name, available from Hitachi Chemical Go. Ltd.) was used for the first, second and third insulating substrates, and that a polymeric epoxy adhesive film AS-3000 (mentioned-above) having a class transition point of about 220°C was used for the first, ் நாள்ளாக அரசு பார்க்கள் and athird interlamination insulating layers நடிய வக்கையை வகரிய கூடி இடிய

The thus produced multilayer wiring boards were proof against exfoliation of laminations and void formation to the initial state, but in a 2-minute solder flow test conducted at 260°C, extellation and void formation took place at many parts in the wiring boards of the Comparative Examples while no such exfoliation and void formation was seen in the wising boards according to the Examples of the present invention.

35 a) r. As described above, the present invention provides a multilayer printed wining board having excellent inhibitory effect against exicilation and yold formation due to heat history of the board and also having high insulation reliability as well as connection reliability of through-holes or via holes, and a process for producing en i i sul-sule i **such a wiring board**egreen i bliw brand genny beliebing sogaleten et gellebong et læssen " i i de provides organism in established demands to an oblaming confronting the sense of an existing the first street

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 depriseCtaims of the problem flumbour graph and or shaped as an experience of the shaped and the contraction of an interest and reposit to see the contraction of the contraction of the contraction A multilayer printed wiring board comprising a plurality of interlaminar insulating layers, a plurality of insubstrates containing a reinforcement, circuits formed on the surface of said insulating subto a 45 mode estrates, and via holes for making electrical connection between two or more layers of circuits, said via the constant holes running through two layers of insulating substrate and an interlaminar insulating layer disposed therebetween; said interlaminar insulating layers being each an insulating layer containing no reinforcement; the B-stage resin flow thereof being less than 1%; and the difference between the glass transition भारत कर के ती । point of each interlaminar insulating layer and that of the adjoining insulating substrate being not greater products 50gaint are than 60°C. gradue that have no such most included adopt the the except

the second of th 2. A multilayer printed wiring board according to Claim 1, wherein the B-stage viscoelasticity of the interlaminar insulating layers is in the range of 2,000-5,000 MPa at 30°C and in the range below 10 MPa at the growth is a few molding temperature. The received in the performance of the minutes of the molding temperature.

the state of the state of the order of the state of the s 3. A multilayer printed wiring board according to Claim 1; wherein cavities for housing semiconductor chips to be mounted later are formed intone or more of the interlaminar insulating layers or the insulating subsuppression of strates. The given the members of the end began each of the price

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- A multilayer printed wiring board according to Claim 1, wherein the cavities are enlarged in size successively from the one in the interlaminal insulating layer or insulating substrate closest to the location where HOUSE DIE. the semiconductor chips are to be set, and terminals for making electrical connection with the semiconmore not be a ductor chips to be mounted later are provided in the circuits formed on the surfaces of the interlaminar insulating layers or insulating substrates exposed by the respective cavities. வுக்கால் கிழுத்தின் க
  - A multilayer printed wiring board according to Claim 4, wherein said cavities are through-holes, and a heat sink is provided closing one of the openings of each of said through-holes.
- 16 16 A'multilayer printed wiring board according to Glaim 3, wherein terminals for making electrical connection with other wiring boards are provided on one side of the board and openings for mounting semiconductor easy the second method are formed in the same side or in the opposite side of the board. ad an end biquation to be GWORLD BY IN A there is all wholes and the entire scenario

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- 7.67 A multilayer printed wiring board according to Claim 6, wherein the terminals for making electrical conad cost 15 for the nection with other wiring boards are pins; the boards and the second .05 E. conditional partitions in the period of the
  - A multilayer printed wiring board according to Claim 6, wherein the terminals for making electrical connection with other wiring boards are lands designed for making electrical connection by solder balls.
- 15 11 120 9 9. 1 A process for producing a multilayer printed wiring board which comprises placing an interlaminar insu-ৈ lating laver between every adjoining thaulating circuit boards having circuits formed on an insulating substrate containing reinforcing floet said interlaminar insufating layer being B-staged, having a B-stage resin flow of less than 1%, with the difference in glass transition point between the adjoining insulating layers being not greater than 60°C, and not containing reinforcing fiber, integrally laminating them by heating under pressure, and forming via holes for making electrical connection between two or more layers of The local end without be and was produced by following the North and the idea in catalants 2 elicepte BRF. and the most stock of the court of the Vertical All Administrations are by a beneficially belong that it was remain
- Aprocess for producing a multilayer printed wiring board which comprises forming an etching resist at the 19 - - - Part where circuit is to be formed on a laminate of copper clad insulating substrates containing reinforcing fiber, etching away the unnecessary copper foil to make an insulating circuit board, preparing at least two pieces of such insufating circuit board; placing an interlaminar insulating layer between said insulating circuit boards, said interlaminal insulating layer being Bustaged, having a Bustage resin flow of less than in the difference in glass transition point between the adjoining insulating layers being not greater than 60°C, and not containing reinforcing (liber, integrally laminating them by heating under pressure, pro-235 to 1211 viding a plating resist over the whole surface of the obtained aminate or illing the laminate to form holes to a depth required for connection, and forming a conductor layer by electroless plating. partition, stage nor on a vine a start training to yundama and the modes between 150
- 11. A process for producing a multilayer printed wiring board which comprises forming an etching resist at the part where circuit is to be formed on a laminate of copper-clad insulating substrates containing reinforcing fiber, etching away the unnecessary copper foil to make an insulating circuit board, preparing at least two pieces of such insulating circuit boards, conducting no circuit working on the outermost surface of the insulating circuit board forming the outermost layer, placing between said insulating circuit boards an inter-ார் ் சிருள்ள ் அளியின் institating layer which is 8-staged; has a B-stage resim flow of less than 1%, with the difference our gold form bus in glass transition point between the adjoining insulating layers being not greater than 60°C, and contains ் 🗟 🔯 🧦 ிக் 🗝 ் no feinfording fiber, Integrally laminating them by heating under pressure; drilling the obtained laminate to supply the conductor layer by electroless plating, forming a plated conductor layer by electroless plating, and the control of the forming an etching resist on the outermost copper surface, and etching away the unnecessary copper. and the Portion of the comment of the least financial for the first tendence for weet the gross translature
- 17 1946 19 12. Aprocess for producing a multilayer printed wiring board which comprises forming an etching resist at the part where circuit is to be formed on a laminate of copper-clad insulating substrates containing reinforcing fiber, etching away the unnecessary copper foil to make an insulating circuit board, preparing at least two சர்கள் கார் அறிக்குpleces of such insulating direuit board placing between said insulating circuit boards an interlaminar inthe State of the sulating layer which is B-staged, has a B-stage resin flow of less than 11%, with the difference in glass transition point between the adjoining insulating layers being not greater than 60°C, and contains no reinforcing fiber, integrally laminating them by heating under pressure, drilling the obtained laminate, forming ாள்க் சுக்கு காக்களை a plated conductor layer by electroless plating to make an interlayer circuit board; preparing at least two ் காரு அளிகள் அறுக்கத் of such interlayer circuit board; placing between said interlayer circuit boards an interlaminar insulating layer which is B-staged, has a B-stage resin flow of less than 1%, with the difference in class

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transition point between the adjoining insulating layers being not greater than 60°C, and contains no reinforcing fiber, integrally laminating them by heating under pressure, providing an etching resist over the whole surface of the obtained laminate, drilling the laminate to form holes to a section where connection is necessary, and forming a plated conductor layer by electroless plating.

- the many of the art. I have the in legislaeta po reychila 13. A process for producing a multilayer printed wiring board which comprises forming an etching resist at the part where interlayer circuit is to be formed on one side of a laminate of copper-clad insulating substrates containing reinforcing fiber, forming an etching resist over the entire surface of the other side, etching away the unnecessary copper foil on the inner layer side to make an insulating circuit board, preparing a pair of such insulating circuit boards, placing therebetween an interlaminar insulating layer which is Bstaged, has a B-stage resin flow of less than 1%, with the difference in glass transition point between the adjoining insulating layers being not greater than 60°C, and contains no reinforcing fiber, integrally laminating them by heating under pressure, drilling the obtained laminate to form holes to a section where connection is required, forming a plated conductor layer by electroless plating, forming an etching resist to the shape of circuit on the copper surface on the inner layer side, forming an etching resist over the entirety of the copper surface on the outer side, etching away the unnecessary copper on the embedded side to make two interlayer circuit poards, placing therebetween an interlaminar insulating layer which is B-staged, has a B-stage resin flow of less than 1%, with the difference in glass transition point between ons maneuru the adjoining insulating layers being not greater than 60°C, and contains no reinforcing fiber, integrally laminating them by heating under pressure, drilling the obtained laminate to form holes to a necessary sussing liquids. The section for connection, forming a plated conductor layer by electroless plating, forming an etching resist 301 doubt 1 doi: to the shape of circuit on the outermost layer, and etching away the unnecessary copper.
- e and the handstales transition countries dithe one with the love of the characteristic panets con-14. The process according to Claim 9, wherein with reference to the B-staged interlaminar insulating layers and the insulating substrates, the difference in glass transition point between the one with the highest ાં દુવા કે કહેલા glass transition point and the ope with the lowest glass transition point is not greater than 30°C.
- on the greaterness with the first production will be the later 1910 for the Library terms of the 15. The process according to Claim 9, wherein the B-stage viscoelasticity of the interlaminar insulating layer colors of the range of 2,000-5,000 MPa at 30°C and in the range below 10 MPa at the molding temperature.
- later against the distribution of the Bushing Citi. The health is the continued to the Line of the Citi. The Co 16. The process according to Claim 9, wherein cavities for housing the semiconductor chips to be mounted and the strategy later are provided in at least one of the B-staged interlaminar insulating layers or the insulating substrates.
- arms in the control of the control of the country of the country of the control of the control of the country o 17.1 The process according to Claim 9, wherein the cavities are enlarged in size successively from the one in the interlaminar ansulating layer or insulating substrate closest to the part for housing the semiconductor chip to be mounted later, and terminals for making electrical connection with the semiconductor chips to be mounted later are provided in the circuits formed on the surfaces of the interlaminar insulating layers the minimum or insulating substrates exposed by the respective cavities, and the cavities of t 30, 5, 5, 6,
  - eto. ny anje 11 up. ikinis of ench tilo ligo noti. 18. The process according to Claim 17, wherein the cavities are through-holes, and a heat sink is provided and the comparation of the openings of each through those of such that the common sections and the common sections of the common sections and the common sections of the common sections and the common sections of the common sections and the common sections are common sections.
- me the indicade forchast and alman smaller in bakings in a filter appoint por our name in 19. The process according to Claim 18, characterized by using a heat sink having a support portion for mountto the line of the semiconductor chips and a brim smaller in thickness than said support portion, forming an opening p. 45. 177 - 9 of substantially the same size as the support portion in the outermost one of the interlaminar insulating and to the many layers or insulating substrates, fitting the supportion of the heat sink in said opening, placing in su-ार कर देश है अपने ह perposed relation the B-staged interlaminar insulating layers, and the insulating circuit boards having circuits formed on an insulating substrate, integrally laminating them by heating under pressure, and forming ார் அத்தார். இது இலுக் holes for making electrical connection between two or more layers of circuits மு
  - povot paugio ache o la que el la la la significação describer de la dissertamente 20. A multilayer printed wiring board according to Claim 10, wherein with reference to the B-staged interlaminar insulating layers and the insulating substrates, the difference in glass transition point between the the control of the sone with the highest glass transition point and the one with the lowest glass transition point is not greater Leville Charles of the Mark Share Charles than 30°C.
- For the time 21.4. The process according to Claim 10, wherein the B-stage viscoelasticity of the interlaminar insulating layers is in the range of 2,000-5,000 MPa at 30°C and in the range below 10 MPa at the molding temperature.

22. The process according to Claim 10, wherein cavities for housing the semiconductor chips to be mounted that a fare are provided in at least one of the B-staged interlaminar insulating tayers or the insulating substrates.

ູ່ແລະ ທີ່ຟາກ ນັກສ້ອນຄວາມປະຕິສິນ ແລະ ສະ ພະ ຄື <del>ປະຕິດ 19 ກອ</del>ວ ປະເ

- 23. The process according to Claim 10; wherein the cavities are enlarged in size successively from the one in the interlaminar insulating layer or insulating layer closest to the part for housing the semiconductor chip to be mounted later, and terminals for making electrical connection with the semiconductor chips to be mounted later are provided in the circuits formed on the surfaces of the interlaminar insulating layers of the insulating layers exposed by the respective cavities.
- # 10 m 24. "The process according to Claim 23, wherein the cavities are through-holes, and a heat sink is provided to what hold closing one of the openings of each through-hole.
- 25. The process according to Claim 24, Characterized by using a fleat sink having a support portion for mounting the semiconductor chips and a brim smaller in thickness than said support portion, forming an opening of substantially the same size as the support portion of said heat sink in the outermost one of the inter-construction of substantially the same size as the support portion of said heat sink in the outermost one of the inter-construction of said heat sink in the outermost one of the inter-construction of the heat sink in said open-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the outermost one of the inter-construction of the heat sink in the inter-construction of the heat sink in the outermost one of the inter-construction of the
- be entropy 26 A multillyer printed wiring board according to Claim 11 Wherein with reference to the B-staged interlating himself insufating layers and the linsufating substrates, the difference in glass transition point between the one with the highest glass transition point and the one with the lowest glass transition point is not greater at the matter of the highest glass transition point and the one with the lowest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transition point is not greater at the matter of the highest glass transiti
- 27. The process according to Claim 11, wherein the B-staged viscoelasticity of the interlaminar insulating layers is in the range of 2,000-5,000 MPa at 30°C and in the range below 10 MPa at the molding temperature.
- ອະການ ເຂົ້າ 28. The process according to Claim 11, Whiterein cavities for housing the semiconductor chips to be mounted 30 later are provided in at least one of the B-staged interlaminar insulating layers or the insulating substrates.
- 29. The process according to Claim 11, wherein the davities are enlarged in size successively from the one in the interlaminar insulating layer or insulating substrate closest to the part for housing the semiconductor encountry. This is to be mounted later, and telminals for making electrical connection with the semiconductor chips to be mounted later are provided in the circuits formed on the surfaces of the interlaminar insulating layers where it is to be mounted by the surfaces of the interlaminar insulating layers of the later and the later are provided by the respective davities of the later and the later

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- 30. The process according to Chaim 29; Whereth the cavities are throught-holes; and a heat sink is provided closing one of the openings of each through-hole.

  The materials are the product seed and the private construction of graduates seem are a few of the constructions.
- 31. The process according to Claim 30, characterized by using a heat sink having alsupport portion for mounting the semiconductor chips and a brim smaller in thickness than the support portion, forming an opening the semiconductor chips and a brim smaller in thickness than the support portion, forming an opening the semiconductor chips and a brim smaller in thickness than the support portion, forming an opening the support portion in the interpolation of said heat sink in said publication in the support portion of said heat sink in said publication opening, placing in superposition the Bistaged interlaminar insulating hayers and the insulating circuit the support of the support portion of said heat sink in said publication opening, placing in superposition the Bistaged interlaminar insulating hayers and the insulating circuit to the support portion of said heat sink in said publication opening. The support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said publication the support portion of said heat sink in said portion to said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said heat sink in said the support portion of said the support portion of said the support portion of said heat sink in said the support port
- 32. The process according to Claim 19, wherein an unevenness for increasing adhesive force is provided on at least the side of the brim portion of the heat sink to be bonded to an insulating layer.
- ethological sectors and process according to Claim 16, wherein terminals for making efectrical connection with other wiring the sectors are provided on one side and openings for mounting the semiconductor chips are formed in the same side or in the opposite side.
  - 34/9The process according to Claim 23/wherein the terminals for making electrical connection with other wirest purposed for boards are processed at the second of the seco

- 35. The process according to Claim 23, wherein lands for making electrical connection by solder balls are provided as terminals for making electrical connection with other wiring boards.
- 36. The process according to claim 9, wherein the laminate molding temperature is 165-200°C.

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37. The process according to Claim 9, wherein at least one of the interlaminar insulating layers or insulating substrates having via holes running therethrough is composed of a thermosetting resin comprising 40-70% by weight of a polyrimide, 15-45% by weight of a polyrimide, 15-45% by weight of an epoxy resin and represented by the following tormula (1):

$$\begin{array}{c|c}
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0
\end{array}$$

$$\begin{array}{c|c}
N & Ar \\
0 & 0 & 0
\end{array}$$

$$\begin{array}{c|c}
1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{array}$$

wherein Ar is a group represented by the following formula (2) or (3), the group of the formula (2) being contained in an amount of 10-98% by mole and the group of the formula (3) being contained in an amount of 90-5% by mole:

wherein Z represents -C(=0)-,  $-SO_2$ -, -O-, -S-,  $-(CH_2)_m$ -, -NH-C(=0)-,  $-C(CH_3)_2$ -,  $-C(CF_3)_2$ -, -C(=0)-O- or a bond; in and m are each an integer of 1 or greater; Z's may be the same or different from each other, and hydrogen in each benzene ring may be substituted with an appropriate substituent;

$$\begin{array}{c|c}
R_1 & & \\
\hline
 & & \\
\hline$$

wherein  $R_1$ ,  $R_2$ ,  $R_3$  and  $R_4$  represent independently hydrogen,  $C_{1-4}$  alky! group or alkoxy group, with at least two of them being alkyl group or alkoxy group; and X represents  $-CH_{2^-}$ ,  $-C(CH_3)_{2^-}$ ,  $-O_-$ ,  $-SO_2$ -, -C(=O)- or -NH-C(=O)-.

50 38. The process according to Claim 16, wherein the openings designed to constitute cavities for housing the semiconductor chips to be mounted later are formed in at least one of the insulating substrates, and the structural members are integrally laminated by heating under pressure to provide a laminate structure of flat panel/protective film combination of B-staged interlaminar insulating layers and insulating circuit boards having circuits formed on insulating substrates/cushion material/molded article having openings of the same size as cavities/flat panel.

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(2)

## FIG.

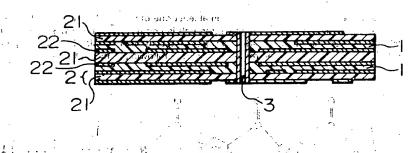
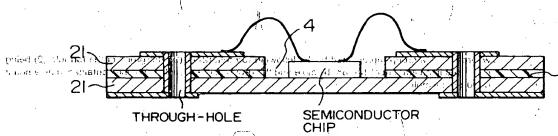
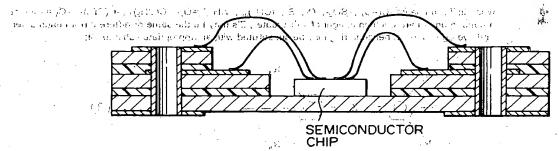


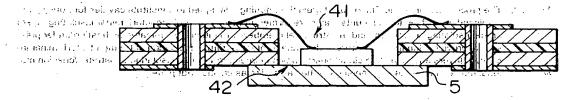
FIG. 2A



## FIG. 2B



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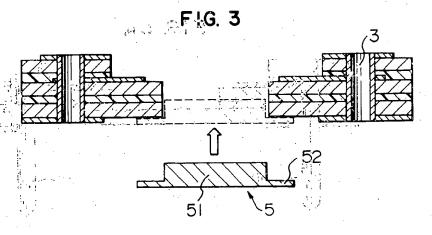


FIG. 4A

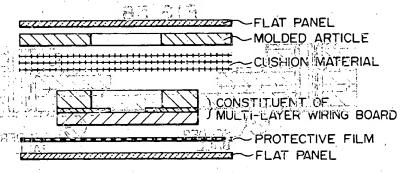
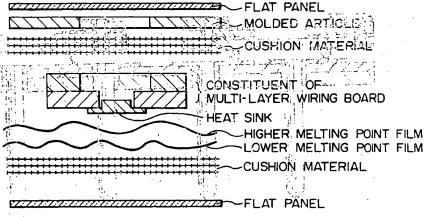
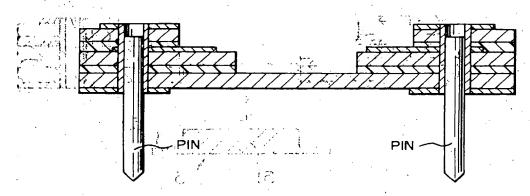


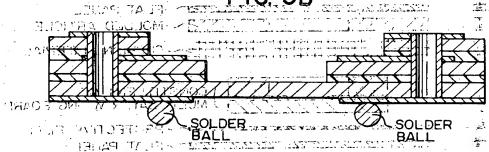
FIG. 4B



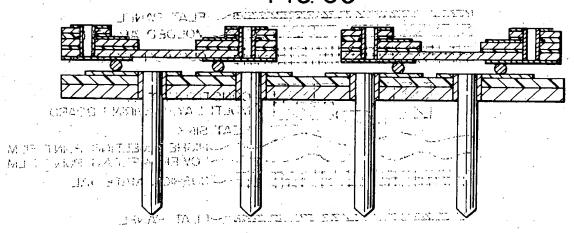
## FIG. 5A



## Λ: 313 F.IG. 5B



## 6 FIG. 5C



| FIG. 6A  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|
| 1 10. 04   | SPOT, FACING WORKING PORTION           |  |  |  |  |  |
| 7777   |  |  |  |  |  |  |
| e e e e e e e e e e e e e e e e e e e  | 71 FIRST SUBSTRATE                     |  |  |  |  |  |
| FIG. 6B  | 723 OPENING                            |  |  |  |  |  |
| d2.45  | 72 FIRST INSULATING LAYER              |  |  |  |  |  |
| FIG. 6C  | 732 INTERNAL CIRCUIT 731 TERMINAL      |  |  |  |  |  |
|  |  |  |  |  |  |  |
| The state of the s | 733 OPENING 73 SECOND SUBSTRATE        |  |  |  |  |  |
| FIG. 6D  | 743 OPENING                            |  |  |  |  |  |
|  |  |  |  |  |  |  |
| FIG. 6E  | 74 SECOND INSULATING LAYER 753 OPENING |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  | 75 THIRD SUBSTRATE                     |  |  |  |  |  |
| FIG. 6F  | 763 OPENING                            |  |  |  |  |  |
| Selver Market  |  |  |  |  |  |  |
|  | 76 THIRD INSULATING LAYER              |  |  |  |  |  |
| FIG. 6G  | 77 FOURTH SUBSTRATE                    |  |  |  |  |  |
| (1) (////  |  |  |  |  |  |  |

FIG. 7

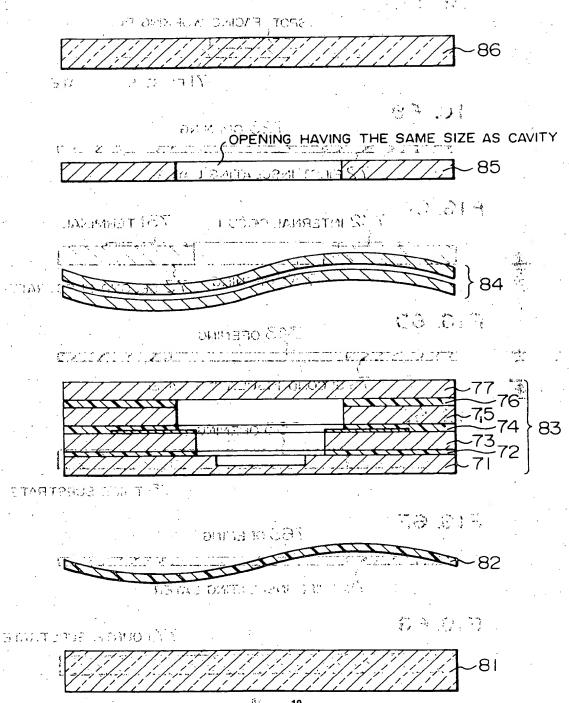
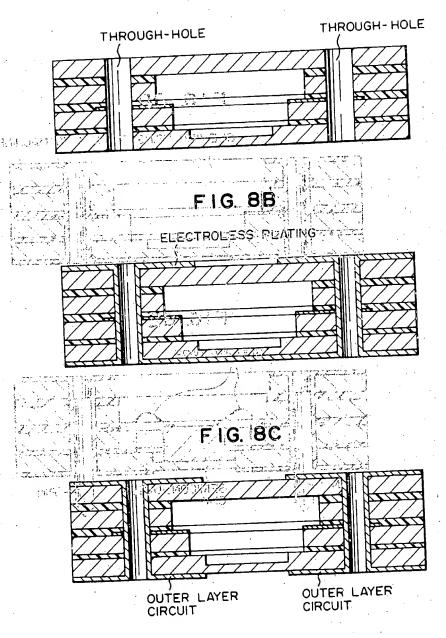


FIG. 8A





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OPENING USING END MILLING MACHINE

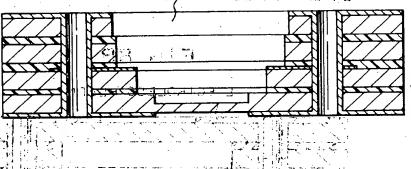
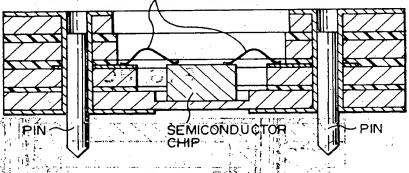
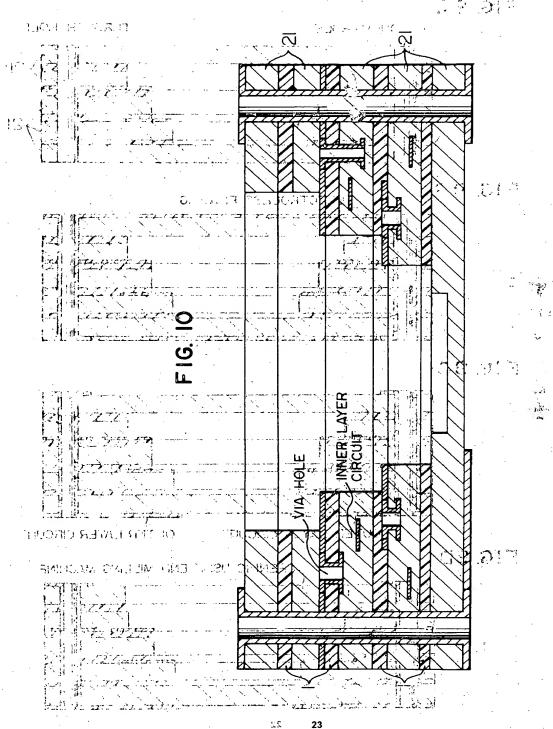


FIG. 8E

BONDING WIRE





## FIG. IIA

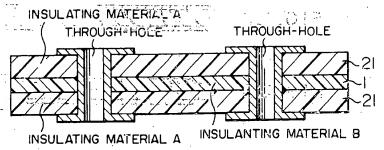


FIG. HE

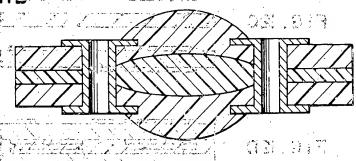


FIG. IIC

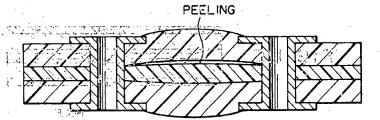
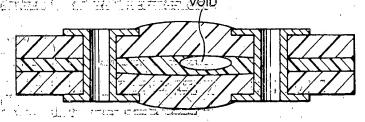
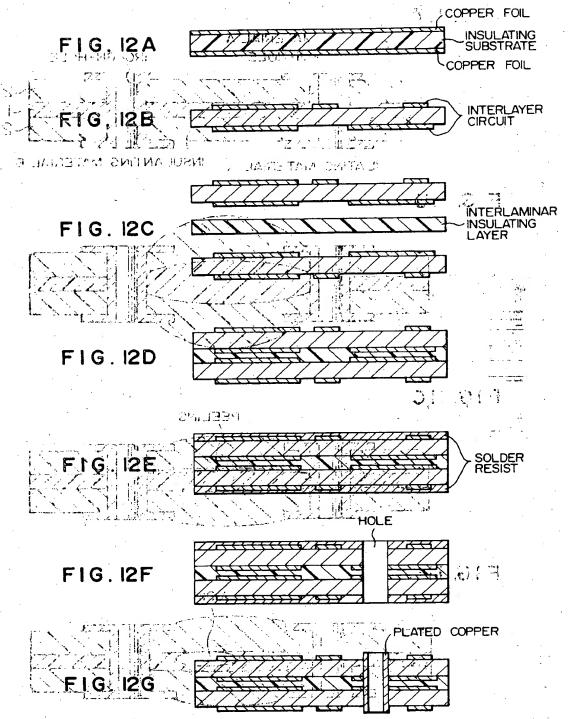
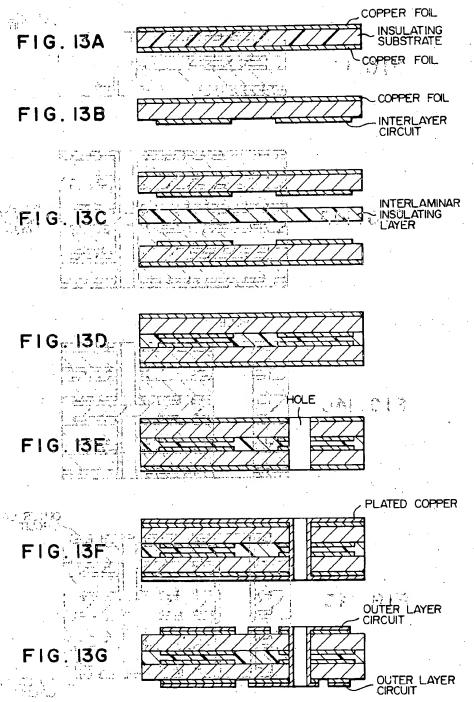
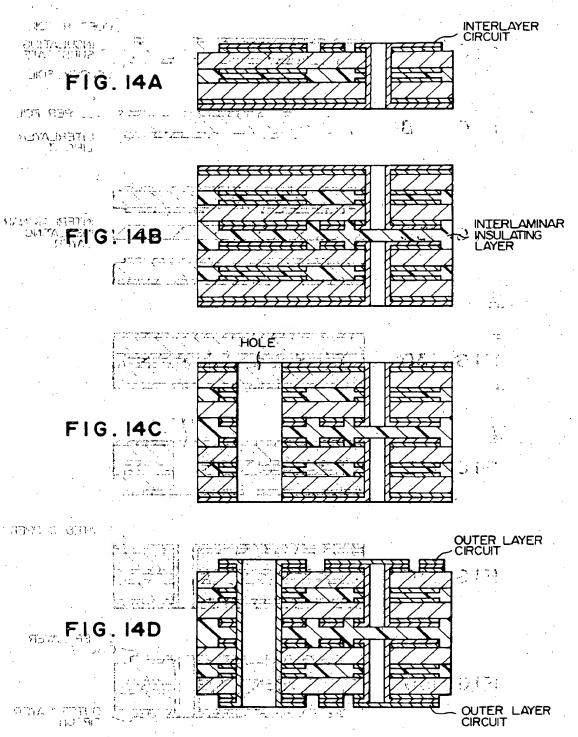


FIG. IID









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# Europäisches Patentamt European Patent Office Office europeen des brevets

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#### **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3: 10.04.1996 Bulletin 1996/15

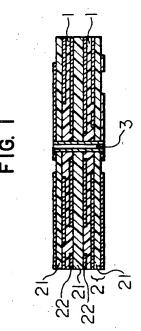
(51) Int CL® **H01L 23/538**, H01L 23/498, H05K 3/46

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#### (54) Multilayer printed wiring board

(57) A multilayer printed wiring board comprising a plurality of interlaminar insulating layers, a plurality of insulating circuit boards having circuits formed on the insulating substrates, and via holes for making electrical connection between two or more layers of circuits, wherein the difference between the glass transition point of an interlaminar insulating layer and that of the adjoining insulating substrate is not greater than 60°C, is proof against exfoliation due to heat history of the board and has high reliability of insulation and through-hole connection.



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## 14 EUROPEAN SEARCH REPORT

Application Number EP 95 30-2211

> ... (32)

| . [  |           | DOCUMENTS CONSIDERED TO BE RELEVAN  |  |   |
|--|-----------|---|--|---|
| - 1  | Category  | Citation of document with indication, where appropriate, of relevant passages   | Relevant<br>to claim   | CLASSIFICATION OF THE APPLICATION (Int.Cl.6)  |
|  | Х         | US-A-3 244 795 (LATIMER) * claims *   | 1,9-13   | H01L23/538<br>H01L23/498<br>H05K3/46  |
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|  |           | The present search report has been drawn up for all claims  |  |   |
|  | S. B. (PO | particularly relevant if taken alone arter the fin  | 96 P. D.   | tion / The state of   |
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